IN THE DRAWINGS

The attached sheets of drawings include changes to Figs. 2 and 8. These sheets, which include Figs. 2 and 8, replace the original sheets including Figs. 2 and 8.

Attachment: Replacement Sheets

REMARKS

Favorable reconsideration of this application is respectfully requested.

Claims 1-22 are pending in this application.[1] Claims 1 and 12 are herein amended.

SUPPORT FOR CLAIM AMENDMENTS

Each of independent claims 1 and 12 now recites a CVD nitride film not extending "above an upper portion of a region that said first gate is formed". That subject matter is supported by Figure 2 in the present specification showing a plurality of gates 8 in a region and the CVD nitride film 14 not extending above any of those gates 8 in the region.

The drawings were objected to. Claims 1-22 were rejected under 35 U.S.C. § 112, second paragraph. Claims 1-4, 7-9, 12-15, and 18-20 were rejected under 35 U.S.C. § 102(b) as anticipated by applicants admitted art. Claims 5, 6, 10, 11, 16, 17, 21, and 22 were rejected under 35 U.S.C. § 103(a) as unpatentable over applicants' admitted art.

Addressing first the objection to the drawings, applicants first note the objection to Figures 19-22 has already been addressed in the Amendment filed April 16, 2008. Specifically, in that amendment replacement Figures 19-22 were submitted, which labeled those figures as --Background Art--.

With respect to the objection to Figures 2 and 8-12, replacement Figures 2 and 8 are submitted herein.

The outstanding drawing objection noted the Figures 2, 7, and 8 appeared inconsistent in that the portion of layer 16 under the gate layer 17 appears to be formed by a different process than the other layer 16 noted in the periphery of Figures 2 and 8.

[1] The present response amends the claims and in the Listing of Claims section shows the amended claims relative to the original U.S. patent 5,945,692. An Appendix is also submitted showing the claim amendments relative to the previously pending claims, as submitted in the Amendment filed April 16, 2008.

In reply to that objection to the drawings applicants note the original labeled element 16 under the gate layer 17 in Figure 2 is now newly labeled element 161, and is noted in the amended specification as formed of silicon oxide. Figure 8 is also herein amended to consistently refer to elements 8 and 7 and delete the original reference indicator "16".

Thereby, the presently submitted replacement Figures 2 and 8 are believed to address the objections to Figures 2 and 8-12.

Addressing now the rejection of claims 1-22 under 35 U.S.C. § 112, second paragraph, that rejection is traversed by the present response.

According to the present invention, a first semiconductor region of a second conductivity type is formed selectively so that a first semiconductor layer remains in an insular form in a central portion of the first major surface of the first semiconductor layer of a first conductivity type.

In the claimed terminology "said first layer remains", the term "remains" indicates the semiconductor layer keeps existing in the portion where the first semiconductor region is not formed, as the first semiconductor region is selectively formed, though initially the first semiconductor layer alone is existing. In addition, the terminology that the first semiconductor layer "remains" in the central portion and peripheral portion of the major surface is recited in the claims because the first semiconductor region is formed on the upper layer of the first semiconductor layer.

Specifically, Figure 3 in the present specification shows the first semiconductor layer 3 remains as an insular region 3 in a center portion of the major surface, and recites the insular region 3 is surrounded by the semiconductor region 5. Figure 3 further shows the first semiconductor layer 3 remains in a ring shape and the peripheral portion of the major surface.

In view of the foregoing amendments and comments applicants respectfully submit each of claims 1-22 is proper under 35 U.S.C. § 112, second paragraph.

Addressing now the above-noted prior art rejections, applicants respectfully submit the claims as written clearly distinguish over applicants' admitted art.

As noted above each of independent Claims 1 and 12 is amended by the present response to clarify the CVD nitride film does not extend above "a region that said first gate is formed", which feature is believed to clearly distinguish over the applied.

The outstanding Office Action is interpreting the admitted art to meet the claim limitations as the layer 14 does not extend above the gate 8 underneath the reference indicator 13. However, that gate 8 underneath the reference indicator 13 is only one gate. As clearly shown in Figure 20 in the present specification the CVD nitride film 14 extends above several of the gates 8 in a region of the gates.

Thereby, applicants respectfully submit no cited art, and particularly not the admitted art, discloses or suggests the claimed features that an integral semi-insulating plasma CVD nitride film does not extend above an upper portion of a region of first gates. With reference to Figure 2 in the present specification as a non-limiting example, the semi-insulating plasma CVD film 14 does not extend above an upper portion of any of the first gates 8.

Further, the applicants of the present invention recognized in the background art such as shown for example in Figures 19 and 20 in the present specification that a structure is known in which a protective film 14 would extend above different gates 8. The applicants of the present invention recognized drawbacks for such a system, discussed throughout the "Description of the Background Art" section of the present application.

The applicants of the present invention in recognizing problems in the background art also recognized a solution to the problems, and particularly the solution being in limiting the extent of the CVD nitride film to not extend above an upper portion of a region that the first gate is formed. Without recognizing the problems in the background art pointed out in the specification, one of ordinary skill in the art would clearly not have been led to any solution

of such problems, and particularly would not have been led to a solution that limits the extent of the CVD nitride film such as in the claims as written.

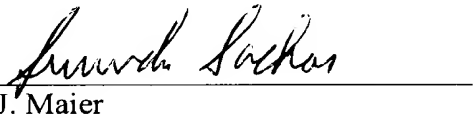
Moreover, the outstanding grounds for rejection is ignoring the fact that the admitted art does not even recognize any problems therein or any solution to such problems. The claimed invention recognized drawbacks in the admitted art and a specific solution of limiting the extent of a CVD nitride film to not extend above an upper portion of a region of a first gate to solve such problems. Applicants submit such a structure is not disclosed in the admitted art and the admitted art does not achieve the benefits realized by the claimed structure.

Thereby, each of independent claims 1 and 12 as currently written is believed to positively recite a structure neither taught nor suggested by the admitted art of Figure 12. Thereby, each of claims 1-22 is believed to be allowable over the noted admitted art.

As no other issues are pending in this application, it is respectfully submitted that the present application is now in condition for allowance, and it is hereby respectfully requested that this case be passed to issue.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



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APPENDIX

Listing of Claims

1. (Currently Amended) A semiconductor device comprising:

a first semiconductor layer of a first conductivity type having first and second major surfaces;

a first semiconductor region of a second conductivity type formed selectively in said first major surface of said first semiconductor layer so that said first semiconductor layer remains along a peripheral portion of said first major surface, and said first semiconductor layer remains in a form of an insular region in a planar view in a central portion of said first major surface;

a second semiconductor region of the first conductivity type formed in a surface of said first semiconductor region, with a channel region provided between said second semiconductor region and said insular region of said first semiconductor layer;

a gate insulating film formed on a surface of said channel region;

a first gate formed on said gate insulating film ~~and formed adjacent said peripheral portion~~;

an interlayer insulating film formed at least on said first gate:

a first main electrode formed over a surface of said interlayer insulating film and covering a surface of said second semiconductor region, said first main electrode being electrically connected to said second semiconductor region and having an end extending to a boundary between the peripheral portion of said first major surface and the central portion of said first major surface;

a second main electrode formed on said second major surface of said first semiconductor layer; and

an integral semi-insulating plasma CVD nitride film covering at least the peripheral portion of said first major surface other than the central portion of said first major surface and not extending above an upper portion of a region that said first gate is formed, said integral semi-insulating plasma CVD nitride film having a conductivity which does not lose function as an insulating film and stabilizes breakdown voltage characteristics of the semiconductor device.

2. (Original) The semiconductor device of claim 1, wherein

said plasma CVD nitride film extends from the peripheral portion of said first major surface to a surface of said first main electrode at said end.

3. (Previously Presented) The semiconductor device of claim 1, further comprising:

a second gate not covered with said first main electrode; and

a gate interconnection line formed selectively on a surface of said second gate,

wherein a trench is formed between said first main electrode and said gate interconnection line for electrical isolation between said first main electrode and said gate interconnect line, and

wherein said first gate and said second gate are integrally formed and electrically connected.

4. (Original) The semiconductor device of claim 3, wherein

said plasma CVD nitride film further extends from a surface of said gate interconnection line through said trench to a portion of a surface of said first main electrode.

5. (Original) The semiconductor device of claim 4, wherein

said plasma CVD nitride film is a semi-insulation film having a conductivity ranging from 1×10^{-14} to 1×10^{-10} ($1/\Omega$cm).

6. (Original) The semiconductor device of claim 4, wherein

said plasma CVD nitride film is a semi-insulation film having a conductivity ranging from 1×10^{-13} to 1×10^{-11} ($1/\Omega$cm).

7. (Original) The semiconductor device of claim 1, further comprising:

a second semiconductor layer of the second conductivity type formed between said second major surface of said first semiconductor layer and said second main electrode.

8. (Previously Presented) The semiconductor device of claim 7, further comprising:

a second gate not covered with said first main electrode; and

a gate interconnection line formed selectively on a surface of said second gate,

wherein a trench is formed between said first main electrode and said gate interconnection line for electrical isolation between said first main electrode and said gate interconnect line, and

wherein said first gate electrode and said second gate electrode are integrally formed and electrically connected.

9. (Previously Presented) The semiconductor device of claim 8, wherein

said plasma CVD nitride film further extends from a surface of said gate interconnection line through said trench to a portion of a surface of said first main electrode.

10. (Original) The semiconductor device of claim 9, wherein

said plasma CVD nitride film is a semi-insulation film having a conductivity ranging from 1×10^{-14} to 1×10^{-10} ($1/\Omega$cm).

11. (Original) The semiconductor device of claim 9, wherein

said plasma CVD nitride film is a semi-insulation film having a conductivity ranging from 1×10^{-13} to 1×10^{-11} ($1/\Omega$cm).

12. (Currently Amended) A semiconductor device comprising:

a first semiconductor layer of a first conductivity type having first and second major surfaces;

at least one first semiconductor region of a second conductivity type formed selectively in said first major surface of said first semiconductor layer so that said first semiconductor layer remains along a peripheral portion of said first major surface, and said first semiconductor layer remains in a form of a plurality of insular regions in a planar view in a central portion of said first major surface;

a plurality of second semiconductor regions of the first conductivity type formed in a surface of said at least one first semiconductor region, with channel regions provided between said second semiconductor regions and said insular regions of said first semiconductor layer;

a gate insulating film formed on a surface of said channel regions;

a first gate formed on said gate insulating film ~~and formed adjacent said peripheral portion~~;

an interlayer insulating film formed at least on said first gate:

a first main electrode formed over a surface of said interlayer insulating film and covering a surface of said second semiconductor region, said first main electrode being

electrically connected to said plurality of second semiconductor regions, said first main electrode further having an end extending to a boundary between the peripheral portion of said first major surface and the central portion of said first major surface;

a second main electrode formed on said second major surface of said first semiconductor layer; and

an integral semi-insulating plasma CVD nitride film for covering at least the peripheral portion of said first major surface other than the central portion of said first major surface and not extending to an upper portion of a region that said first gate is formed, said integral semi-insulating plasma CVD nitride film having a conductivity which does not lose function as an insulating film and stabilizes breakdown voltage characteristics of the semiconductor device.

13. (Original) The semiconductor device of claim 12, wherein

said plasma CVD nitride film extends from the peripheral portion of said first major surface to a surface of said first main electrode at said end.

14. (Previously Presented) The semiconductor device of claim 13, further comprising:

a second gate not covered with said first main electrode; and

a gate interconnection line formed selectively on a surface of said second gate,

wherein a trench is formed between said first main electrode and said gate interconnection line for electrical isolation between said first main electrode and said gate interconnect line, and

wherein said first gate and said second gate are integrally formed and electrically connected.

15. (Original) The semiconductor device of claim 14, wherein

said plasma CVD nitride film further extends from a surface of said gate interconnection line through said trench to a portion of a surface of said first main electrode.

16. (Original) The semiconductor device of claim 15, wherein

said plasma CVD nitride film is a semi-insulation film having a conductivity ranging from 1×10^{-14} to 1×10^{-10} ($1/\Omega$cm).

17. (Original) The semiconductor device of claim 15, wherein

said plasma CVD nitride film is a semi-insulation film having a conductivity ranging from 1×10^{-13} to 1×10^{-11} ($1/\Omega$cm).

18. (Original) The semiconductor device of claim 13, further comprising:

a second semiconductor layer of the second conductivity type formed between said second major surface of said first semiconductor layer and said second main electrode.

19. (Previously Presented) The semiconductor device of claim 18, further comprising:

a second gate not covered with said first main electrode; and

a gate interconnection line formed selectively on a surface of said second gate,

wherein a trench is formed between said first main electrode and said gate interconnection line for electrical isolation between said first main electrode and said gate interconnect line, and

wherein said first gate and said second gate are integrally formed and electrically connected.

20. (Original) The semiconductor device of claim 19, wherein

said plasma CVD nitride film further extends from a surface of said gate interconnection line through said trench to a portion of a surface of said first main electrode.

21. (Original) The semiconductor device of claim 20, wherein

said plasma CVD nitride film is a semi-insulation film having a conductivity ranging from 1×10^{-14} to 1×10^{-10} ($1/\Omega$cm).

22. (Original) The semiconductor device of claim 20, wherein

said plasma CVD nitride film is a semi-insulation film having a conductivity ranging from 1×10^{-13} to 1×10^{-11} ($1/\Omega$cm).